PhD position

Generation of Dedicated Microprocessors by Generative AI

Keywords: Electronic design automation, Generative AI, Processor architecture, RISC-V instruction set

1 Introduction and Context

The main advantage of the RISC-V instruction set architecture is that it facilitates the emergence of new players in the processor world. Indeed, the fact that this architecture is open and royalty-free allows for customization and/or variations without licensing fees. This diversity should foster innovation in the design of new processor architectures. Adding a hardware accelerator to a RISC-V processor architecture offers several significant advantages, particularly when it comes to improving performance for specific tasks while maintaining flexibility. The main benefits of this approach are:

- Improved performance of a general-purpose processor for highly specific operations;
- Offloading critical operations so the processor can focus on more general-purpose tasks or on controlling the overall execution of a program;
- Customization of processor architectures to specific application domains;
- Control of the RISC-V processor's throughput, latency, and power consumption.

In this context, one of the challenges is making new software tools available to the community to help in processor design. These tools must both facilitate collaboration between designers and accelerate the development of new processor variants.

The exploitation of the potential of generative AI in defining new design methodologies [1] and associated tools is the subject of recent researchs. Among these, we can cite the automatic generation of integrated circuit placement/routing using reinforcement learning [2] or the use of a large language model (LLM) for exploring the space of dedicated architectural solutions [3]. At the algorithmic level, there is, for example, research [4] aimed at identifying efficient matrix multiplication algorithms using deep reinforcement learning. More specifically regarding processors, initial work by [5] examined the feasibility of using language models such as ChatGPT to generate VHDL code describing a RISC processor core. This work highlights the current strengths and limitations of this approach. Furthermore, a study presented in [6] explores the challenges and opportunities encountered when using LLM to generate test vectors, both to facilitate testability and to ensure comprehensive test coverage during the validation of processor architectures.

2 Scientific Objectives

Therefore, leveraging a large Language Model Language (LLM) to automate the customization of a RISC-V processor architecture seems an innovative approach that opens further exploration. Indeed, LLMs can help identify and integrate specific instructions for application domains such as artificial intelligence, image processing, digital communications, and cryptography. By interpreting the needs of end users or application developers, an LLM can propose tailored instruction extensions that meet the specific requirements of the target domains. Furthermore, it can facilitate the automation of the hardware and software co-design involved in implementing a particular variant of a RISC-V processor architecture.

3 Candidate Profile

The candidate must hold a Master's degree (or equivalent) and must be able to demonstrate theoretical and practical knowledge in the following areas:

- Knowledge of processor architecture
- Knowledge of generative AI and large-scale modeling languages
- Familiarity with hardware description languages (VHDL, SystemVerilog)

4 Thesis Context

This PhD project is part of the CADabrIA action within the PEPR PHOENIX program. This action lies at the intersection of computer science (machine architectures) and machine learning. The doctoral candidate will be fully integrated into the project (discussions, meetings, seminars) and will collaborate with other participating researchers and doctoral/Master's students. He/she will have the opportunity to co-supervise interns. Teaching opportunities (paid in addition to their salary) may be offered.

This project is a collaboration between the ASIC team at the CNRS IETR laboratory and the CSN team at the CNRS IMS laboratory. The ASIC team brings its expertise in circuit design and design methodology with the doctoral candidate. The CSN team will contribute its expertise in FPGA/ASIC design of flexible processors based on RISC-V ISAs. The successful candidate will be based at the IETR laboratory's Nantes site. It will also be expected to spend time at the IMS laboratory during periods of its doctoral research.

- **Research Laboratories:** IETR (UMR CNRS 6164), IMS (UMR CNRS 5218)
- **University:** Nantes University
- **Location:** IETR/Polytech, Nantes, FRANCE
- **Expected Start Date:** September or October 2026 (3-year duration)

5 Application

Applications must be submitted exclusively via the AMETHIS platform. Applications received outside the AMETHIS process will not be considered.

For more information, please contact:

- **Prof. Sébastien Pillement**, sebastien.pillement@univ-nantes.fr ,
- **Prof. Christophe Jégo**, christophe.jego@ims-bordeaux.fr .

Applications will be reviewed as they are received. Interviews will be held after the application period. Applications that do not meet the qualifications will not be considered for interviews.

Since integration into the IETR laboratory requires access to a restricted, secure area, we ask that you allow sufficient time for the review of your profile if you wish to apply. This process can take up to two months.

References

[1] Zhuolun He et al. "Large language models for eda: Future or mirage?" In: *ACM Transactions on Design Automation of Electronic Systems* 30.6 (2025), pp. 1–53.

[2] Azalia Mirhoseini et al. "A graph placement methodology for fast chip design". In: *Nature* 594.7862 (2021), pp. 207–212.

[3] Kaiyan Chang et al. "Chipgpt: How far are we from natural language hardware design". In: *arXiv preprint arXiv:2305.14019* (2023).

[4] Alhussein Fawzi et al. "Discovering faster matrix multiplication algorithms with reinforcement learning". In: *Nature* 610.7930 (2022), pp. 47–53.

[5] Shadeeb Hossain et al. "Using llm such as chatgpt for designing and implementing a risc processor: Execution, challenges and limitations". In: *arXiv preprint arXiv:2401.10364* (2024).

[6] Chao Xiao et al. "Llm-based processor verification: A case study for neuromorphic processor". In: *2024 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE. 2024, pp. 1–6.